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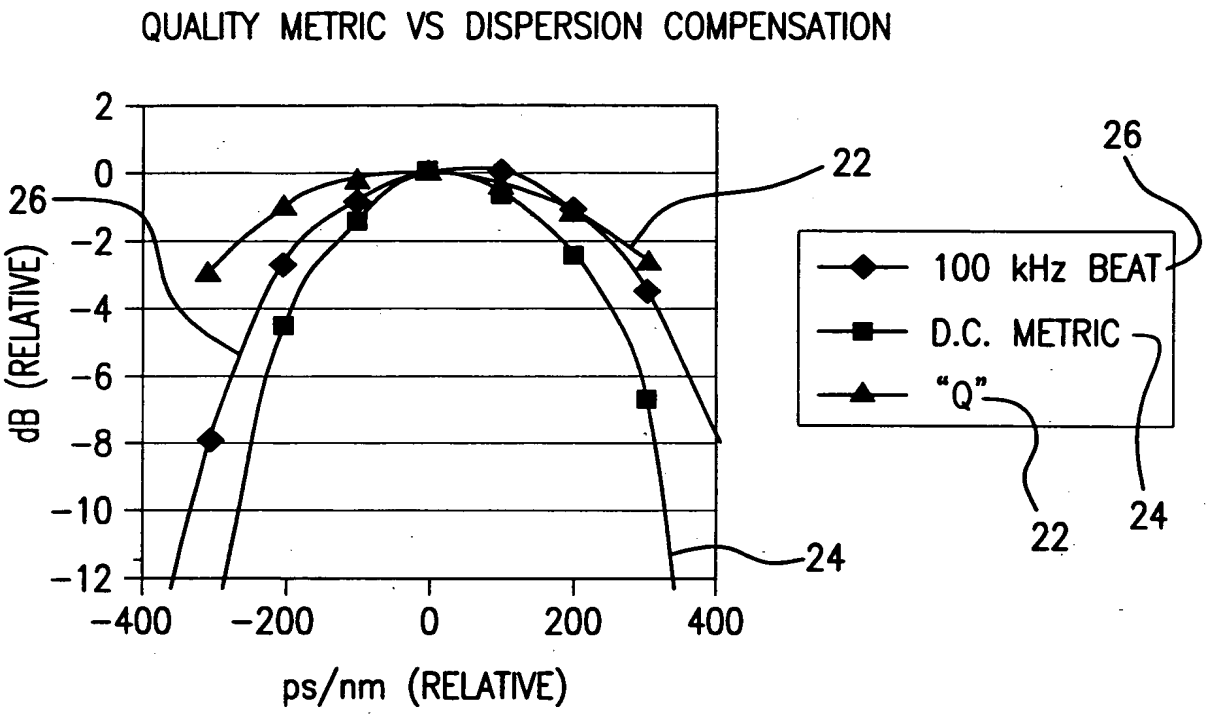


FIG. 1

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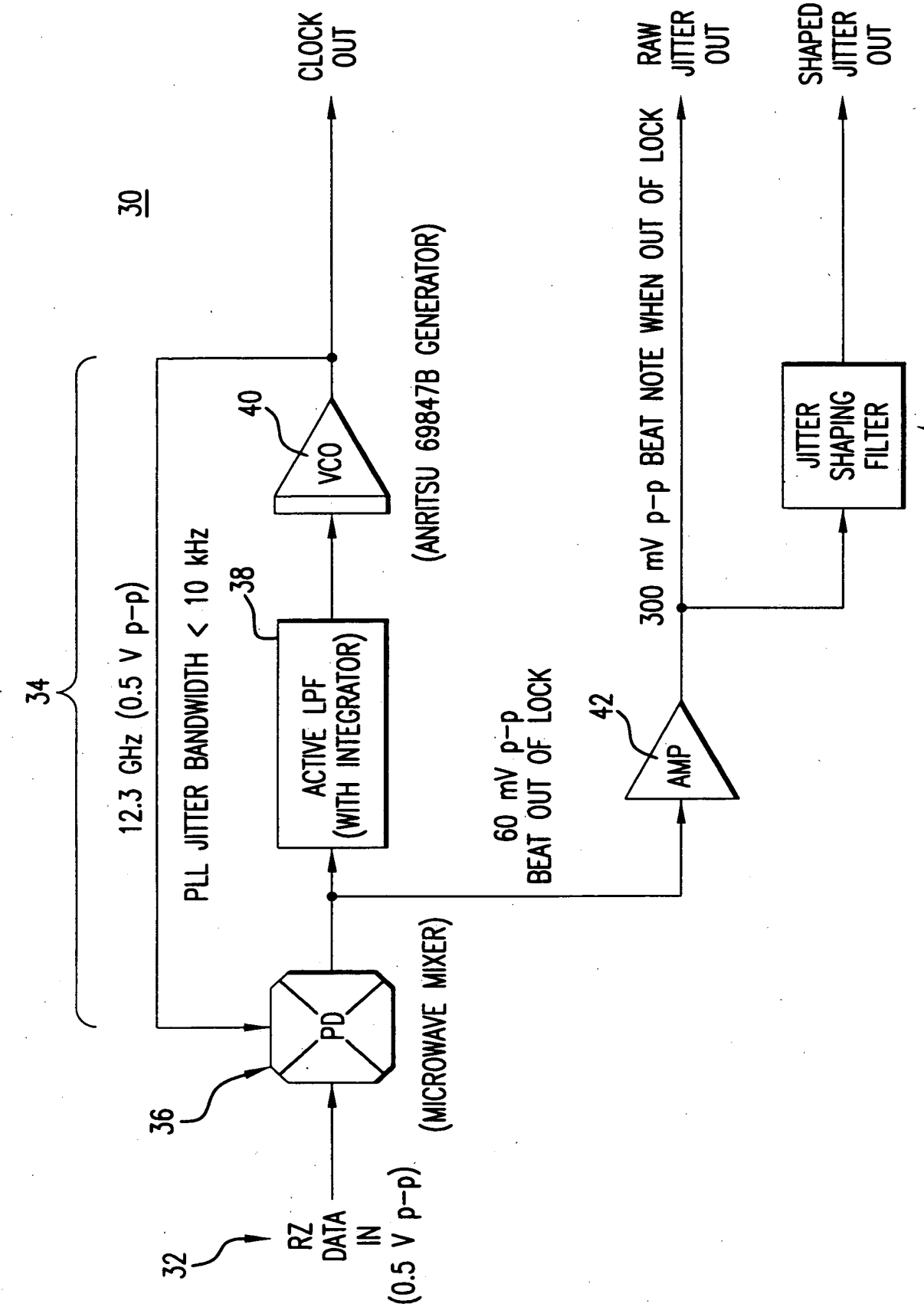


FIG.2

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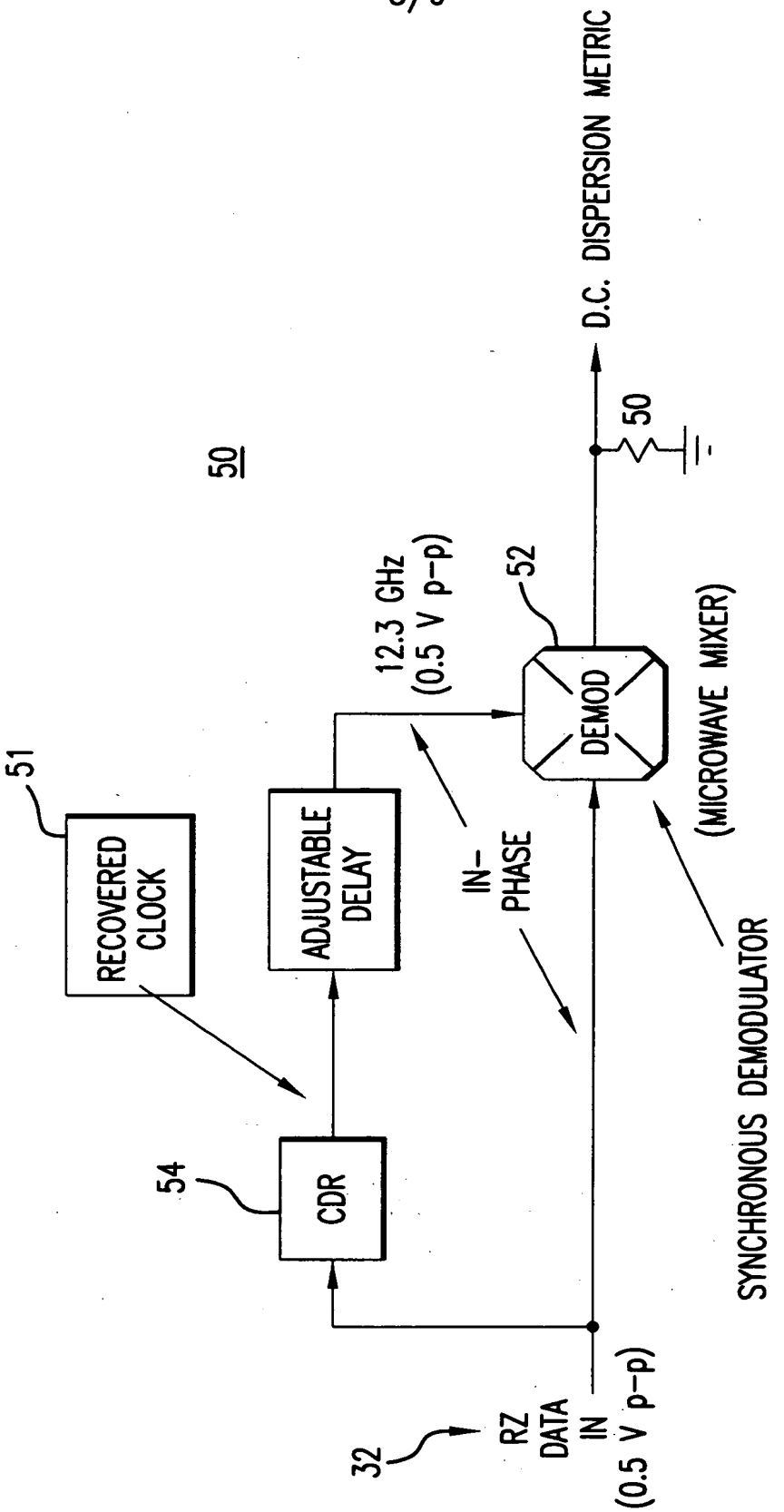


FIG.3

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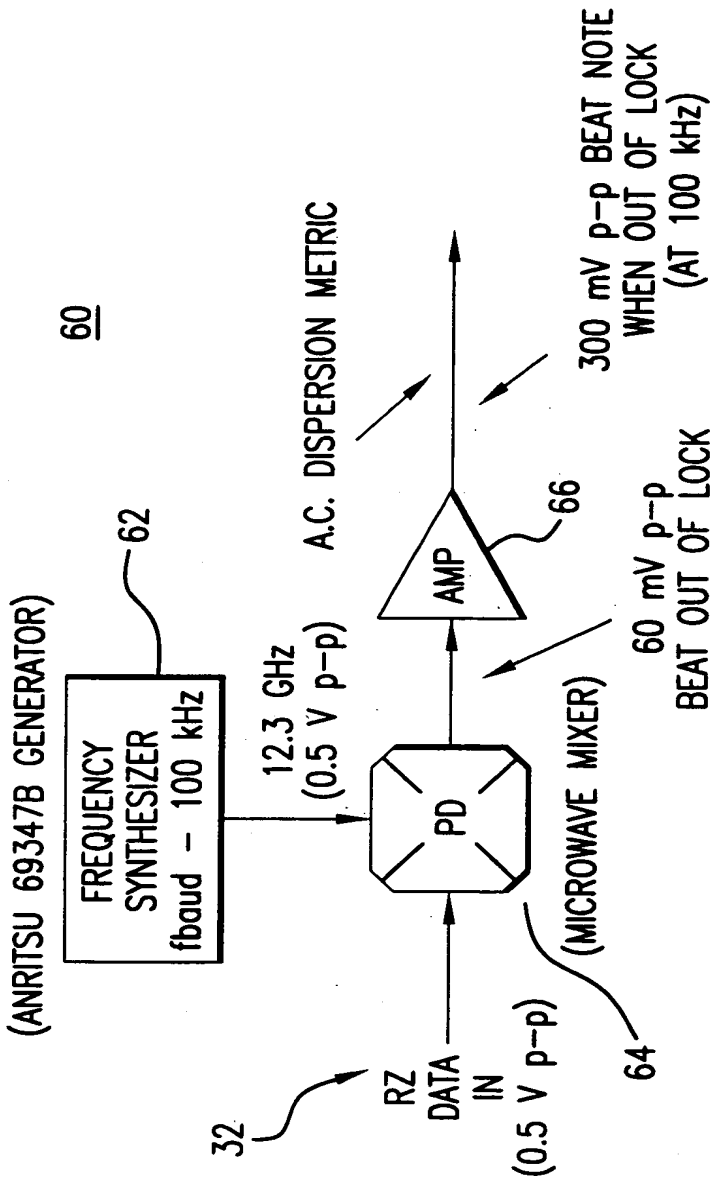


FIG.4

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JC67



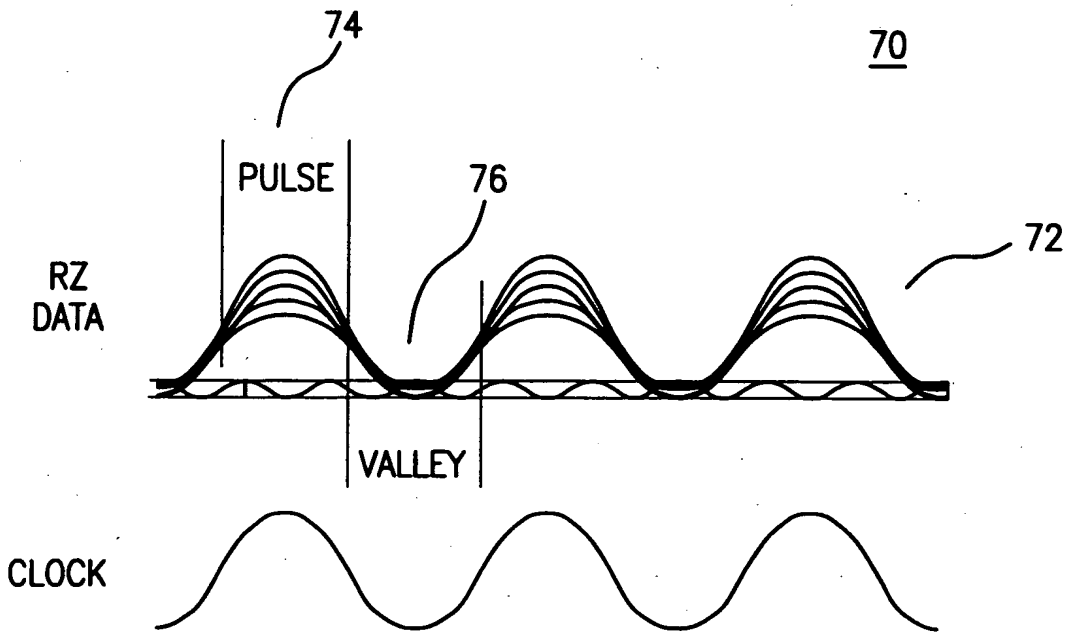


FIG.5

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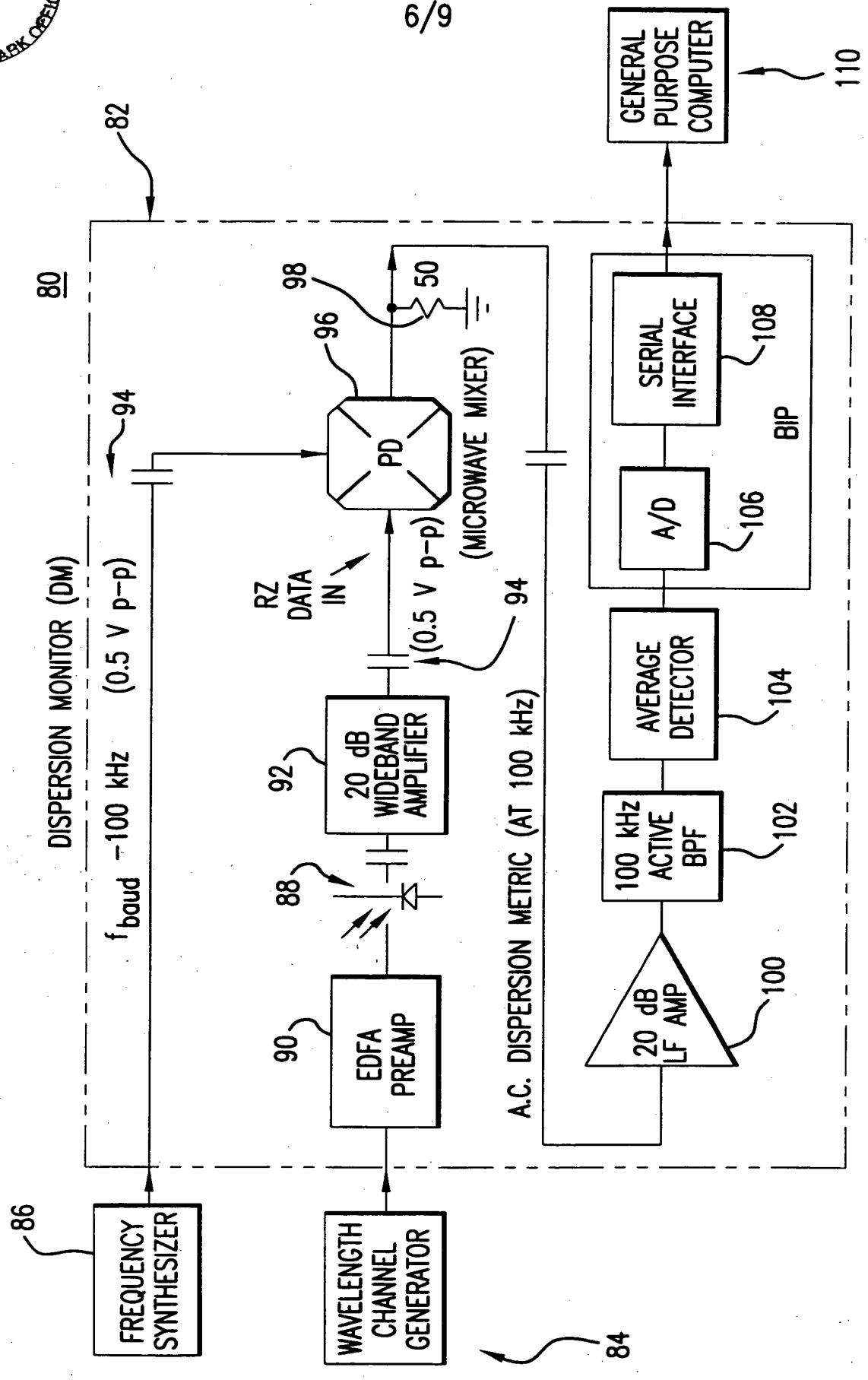


FIG.6

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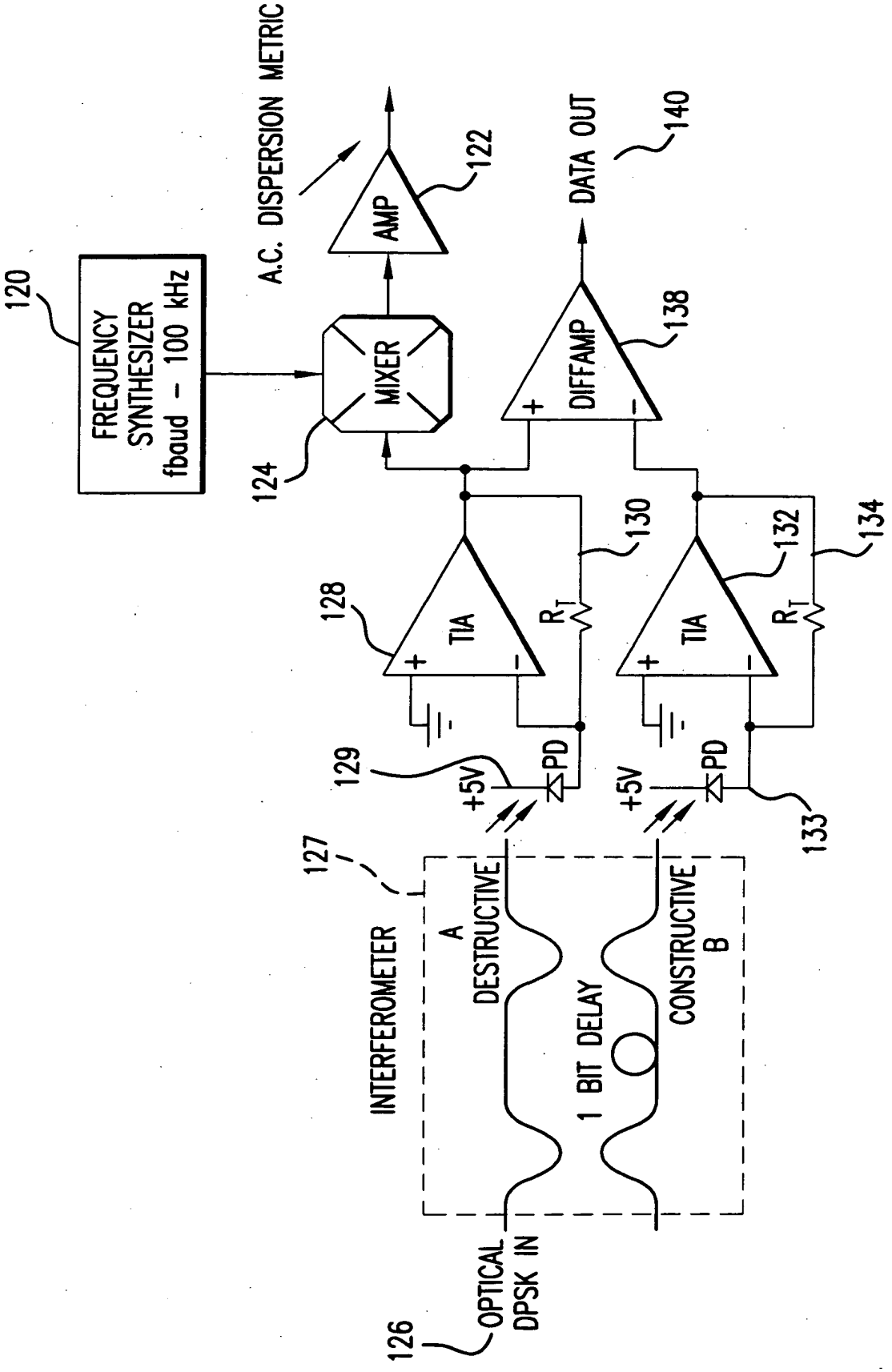


FIG. 7

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TRADITIONAL PLL (PHASE-LOCKED LOOP) CIRCUIT WITH ERROR SIGNAL TO VCO DISABLED

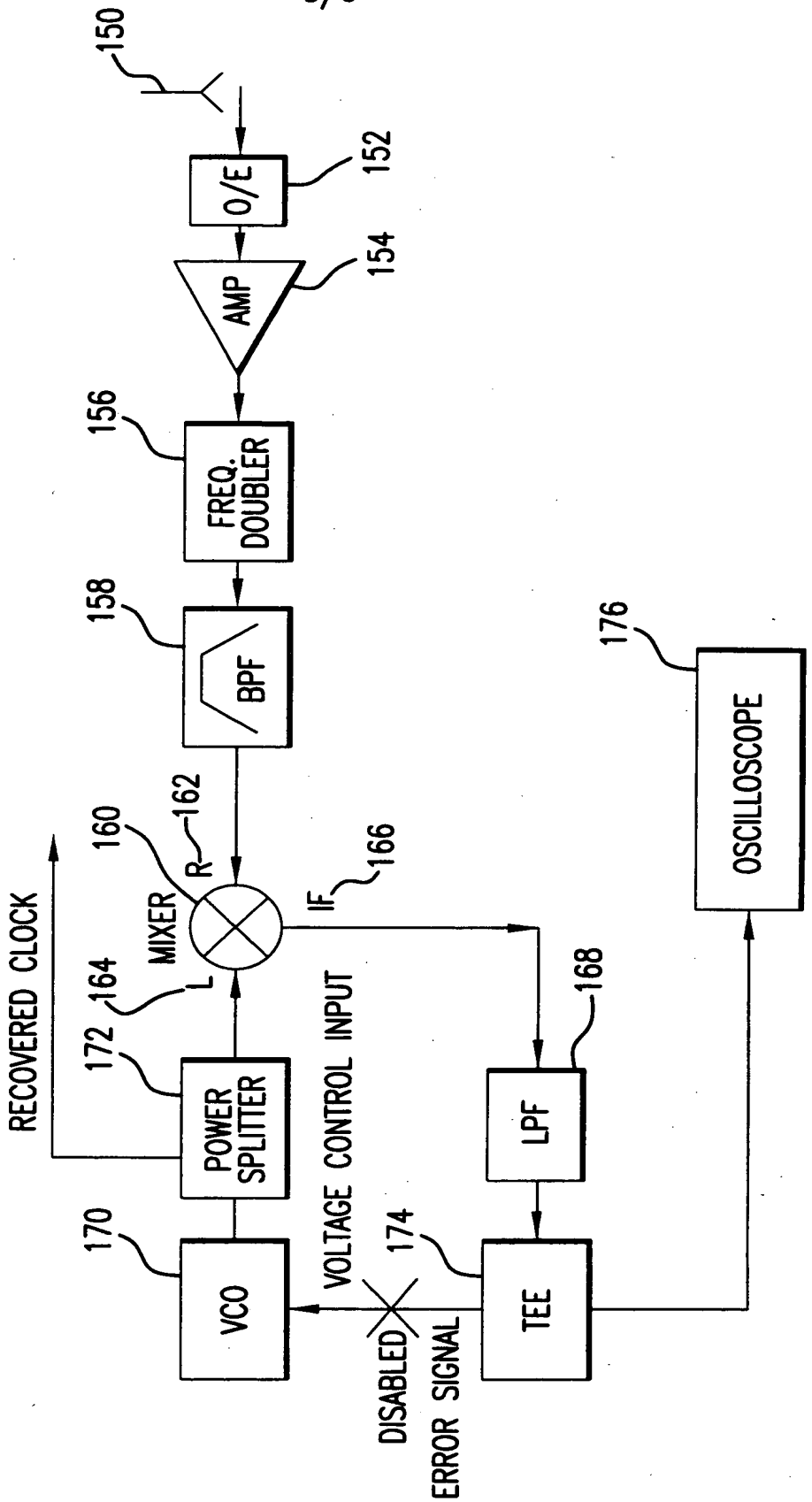


FIG.8

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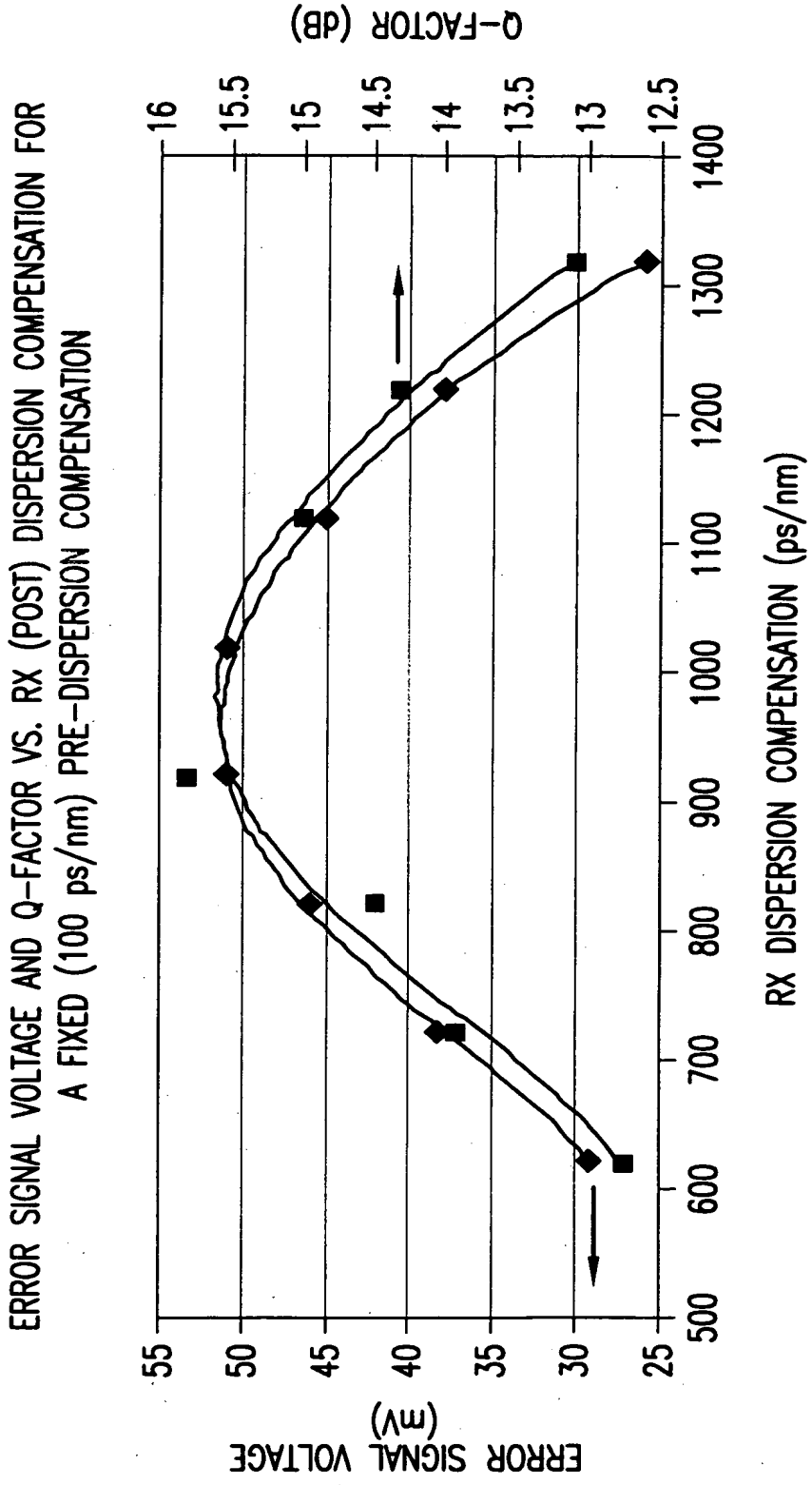


FIG.9